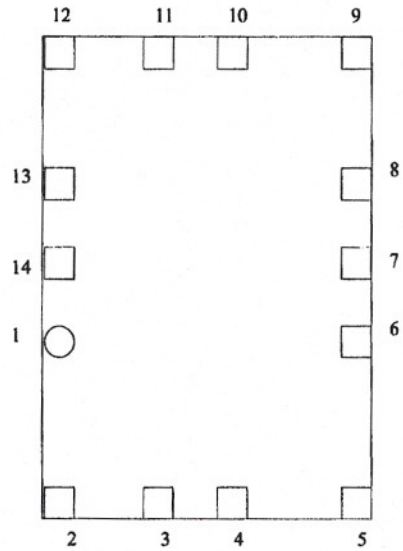
ISO9001:2000 Certified SCI Quality System

Sierra Components, Inc.

2222 Park Place Building 3 Suite E • Minden, Nevada 89423
Phone: 775.783.4940 Fax: 775.783.4947

QUAD CMOS 2 INPUT OR GATE



PAD FUNCTIONS

1. INPUT A1
2. INPUT B1
3. OUTPUT Y1
4. OUTPUT Y2
5. INPUT A2
6. INPUT B2
7. VSS
8. INPUT A3
9. INPUT B3
10. OUTPUT Y3
11. OUTPUT Y4
12. INPUT A4
13. INPUT B4
14. VDD

NOTE: BONDING PAD ON DIE PIN 7 HAS ROUNDED CORNERS

The information given is believed to be correct at the time of issue.
Please verify your requirements prior to commencement of any assembly process, as no liability for omission or error can be accepted.
Chip back potential is the level at which bulk silicon is maintained either by bond pad connection or in some cases the potential to which the chip back must be connected if stated above.

Note: 1 mil = 0.001inch

APPROVED NM ..... DATE: 06/12/2006	CD4071B NATIONAL SEMICONDUCTOR	DIE INFORMATION DIMENSIONS (Mils): 54 x 40 BOND PADS (Mils): MASK REF: GEOMETRY: REV A BACK POTENTIAL:
SERIAL NUMBER. 001073		METALLISATION TOP: Al BACK: Si